REMARKS

This paper is responsive to Office Action dated December 15, 2004. Claims 1-28 were examined. None of the claims have been amended and no new claims have been added. Applicant respectfully traverses all rejections.

Rejections under 35 U.S.C. §103

Hetzler in view of Watts

Claims 1, 3-11, 13-24 and 26-28 are rejected under 35 U.S.C. §10 3(a) as being unpatentable over U.S. Patent No. 5,954,820 issued to Hetzler (hereinafter "Hetzler") in view of U.S. Patent No. 5,218,704 issued to Watts (hereinafter "Watts"). Applicant traverses the rejections because 1) Hetzler discloses multiple power levels for a CD-ROM drive and does not disclose or suggest performance states of an integrated circuit, 2) Watts does not disclose or suggest comparing a determined integrated circuit's utilization level with a threshold contrary to the assertion by the Office, 3) Hetzler does not disclose instruction sequences as recited in Applicant's claims contrary to the Office's assertion, and 4) the combination of the references still does not disclose or suggest Applicant's claims, regardless of whether such combination is appropriate.

1) Hetzler discloses multiple power levels of a CD-ROM drive

Although Hetzler discloses skipping an intermediate mode (IDLE2-power save) to a maximum operation mode (SEEK/READ) as depicted in Table 2 at column 7, lines 5 – 15, the operational/power modes of a CD-ROM drive are not performance states of an integrated circuit. Hetzler discloses controlling power levels of two components of a notebook computer: the CD-ROM drive and the LCD display. The only component disclosed in Hetzler with multiple power levels is the CD-ROM drive. The LCD display only has two modes or power values as depicted in Table 1 at column 5, lines 59 – 65. Hetzler does not disclose or suggest skipping intermediate performance states for an integrated circuit, and only discloses skipping an intermediate power level of a CD-ROM drive. Furthermore, Watts' disclosure is limited to only 2 performance states for its central processing unit (active and resting). Neither of the references, standing alone or in combination, discloses or suggests skipping intermediate performance states of an

integrated circuit or an integrated circuit with multiple performance states including a maximum performance state and multiple lesser performance states.

2) Watts does not disclose or suggest comparing a determined utilization level to a threshold value

The Office admits that Watts does not explicitly disclose or suggest comparing an integrated circuit's determined utilization level to a threshold value. The Office then asserts that it would be obvious to make such a comparison "because the value representing the utilization is worthless by itself and therefore requires at least one other value in which to compare it to...." Watts does make a comparison of the determined activity level with another value, but the value is a previous determined activity level and not a threshold value. Watts discloses determining a CPU activity level and then aligning a T(off) interval based on whether the determined activity level has increased or decreased since the previous determination of activity level (col. 5, lines 60 – 66; Figure 1). The previously determined activity level is not a threshold value, and the comparison of the two determined activity levels in Watts does not cause the CPU to enter a predetermined performance state. The comparison of determined activity levels in Watts is utilized for aligning the T(off) interval. Claim 1 recites "comparing the determined utilization to a threshold utilization value; and if the determined utilization is above the threshold, entering a predetermined performance state as a next performance state..." and claim 19 recites "means for comparing the utilization to a first threshold utilization value and for always changing operation ...in response to a determination that the utilization is above a threshold utilization value." Neither of these claims are disclosed or suggested by Hetzler or Watts, standing alone or in combination.

3) The prior art of record does not disclose or suggest instruction sequences as recited in Applicant's claims

The Office refers to column 25, lines 51 – 58 of Hetzler to supports its rejection of claims 11 and 23. Applicant notes that claims 16 and 26 also recite instruction sequences that are not disclosed or suggested by either of Hetzler or Watts. The section cited by the Office states that "the program instructions for implementing the invention, as shown by the flow charts in FIGS. 3, 5 – 7 and 11 – 12, may be stored as microcode...." None of these figures disclose the subject

matter of claims 11, 16, 23, or 26. The following is the brief description of the figures from the cited section:

> FIG. 3 is a flow chart illustrating the **counting of accesses** to one or more power-consuming components within a predetermined time window.
> FIG. 5 is a flow chart illustrating **computation of the access frequency** and comparison to a threshold frequency for determining when to enter a disk drive power-save mode.
> FIG. 6 a flow chart illustrating the **computation of the threshold frequency** using prior access frequencies stored in a ring buffer.
> FIG. 7 a flow chart illustrating the **computation of the threshold frequency** using prior access densities stored in a ring buffer.
> FIG. 11 is a flow chart illustrating the **computation of the energy/response** and missed opportunity penalties when a power-save mode is exited.
> FIG. 12 is a flow chart illustrating the **computation of the cumulative missed opportunity penalty** and adjustment of the gain factors when the trip level is crossed.

From their descriptions, it can be seen that the Figures do not illustrate changing performance state of an integrated circuit as recited in claims 11, 16, 23, and 26, or skipping performance states as recited in claims 11 and 23.

4) Combination of references still does not disclose or suggest Applicant's claims

Applicant respectfully submits that, if such combination of modification is appropriate, then combining or modifying Hetzler with Watts still fails to achieve Applicant's claimed invention. Modifying or combining Hetzler with Watts may result in appending Watts' technique of placing a aligning a T(off) and placing a CPU either in an active or rest state to Hetzler's technique of exiting or entering power save mode for a CD-ROM drive. Hence, combining or modifying Hetzler in view of Watts does not achieve any of Applicant's claims.

5) Dependent claims

With regard to claims 7 and 14, the Office rejects these claims on the basis that "Watts teaches that the power mode can be adjusted by changing the frequency of the CPU." However, claim 7 recites "wherein the performance state is reduced by both reducing both voltage and clock frequency of the integrated circuit," and claim 14 recites "wherein each of the performance

states is defined by a unique voltage and frequency combination." The Office fails to indicate support for rejection of the combination of frequency and voltage or reduction of both frequency and voltage.

With regard to claims 18 and 28, the Office refers to rejections of claims 1 – 2 and 4 – 11. However, there are no claims in claims 1 – 2 and 4 – 11 that correspond to claims 18 and 28.

Hetzler, Watts, and Kawata

Claims 2, 12 and 25 are rejected under 35 U.S.C. §10 3(a) as being unpatentable over Hetzler and Watts as applied to claims 1, 3-11, 13-24 and 26-28 above, and further in view of U.S. Patent No. 6,076,171 issued to Kawata (hereinafter "Kawata"). The Office cites to Figures 15 and 17, and column 16, lines 32 – 56 of Kawata to reject claims 2, 12, and 25. These figures and lines disclose a flow chart for controlling operation of a CPU and a transition table of CPU clock states. These sections disclose stepping through performance levels until arriving at a sufficient performance level. There is no disclosure in Kawata of entering a target performance state that is a near maximum performance state as recited in claims 2, 12, and 25.

In summary, claims 1 – 28 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Steven R. Gilliam — 15-May-2005 (Date)

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Respectfully submitted,

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